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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,872	05/31/2001	Richard P. Mackey	10559-389001	1080

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EXAMINER
PUENTE, EMERSON C

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/872,872	MACKEY ET AL.
	Examiner	**Art Unit**	
	Emerson C Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _24 January 2005_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-6 and 13-21_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _17-20_ is/are allowed.

6)☒ Claim(s) _1-6,13-16 and 21_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _31 May 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.

4)☐ Interview Summary (PTO-413) Paper No(s). _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: .

DETAILED ACTION

This action is made **Non-Final**.

Claims 1-6 and 13-21 have been examined.

Claims 7-12 have been canceled.

Claim Objections

Claim 15 objected to because of the following informalities:

In regards to claim 15, please change "the power fail controller" to "a power fail

controller" to avoid lack of antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by US

Patent No. 5,182,687 of Campbell et al. referred hereinafter "Campbell".

In regards to claim 1, Campbell discloses:

detecting a reset condition (see column 17 lines 35-42);

verifying a memory controller is initialized by determining if a reset signal is detected for

a predetermined period of time (see column 18 lines 1-15); and

placing a memory system into a self-refresh mode using a state machine in the memory

controller. Campbell discloses input to a reset circuit, which changes states to produce a reset

signal to reset the processor, indicating using a state machine in the memory controller (see column 17 lines 53 to column 18 lines 15). Campbell further discloses being able to resume operations to a known condition when power is restored (see column 18 lines 49-51), thus indicating placing a memory system into a self-refresh mode.

In regards to claim 2, Campbell discloses verifying the memory controller is initialized by delaying a reset signal (see column 18 lines 9-15).

In regards to claim 3, Campbell discloses monitoring the voltage level of a system to determine a power (see column 17 lines 35-42).

In regards to claim 4, Campbell discloses generating a reset condition when either a power failure or a reset request occurs (see column 17 lines 35-42 and column 18 lines 35-40).

In regards to claim 5, Campbell discloses verifying the reset request does not occur prior to initialization (see column 18 lines 9-15).

In regards to claim 6, Campbell discloses detecting the reset condition and verifying the memory controller is initialized external to the memory controller (see column 18 lines 9-15).

In regards to claim 13, Campbell discloses wherein the detecting a reset condition detecting either a power failure or reset signal (see column 17 lines 38-42);

generating a delay signal based on the reset signal (see column 18 lines 9-15); and

initiating a data self-refresh routine if the delay signal indicates the memory system is initialized (see column 18 lines 9-15 and 35-50).

In regards to claim 14, Campbell discloses monitoring the voltage level of a system to determine a power failure (see column 17 lines 35-42 and column 18 lines 35-40).

In regards to claim 15, Campbell discloses generating two output signals by the power

fail controller to the state machine controller based on the reset signal (see figure 9a item 270

and 234 and column 17 lines 40-50 and column 18 lines 5-15).

In regards to claim 16, Campbell discloses preventing initiating the data self-refresh

routine if the reset signal is not asserted for a predetermined period of time (see column 17 lines

53 to column 18 line 15).

Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No.

4,777,626 of Matsushita et al. referred hereinafter "Matsushita".

In regards to claim 21, Matsushita discloses:

monitoring a voltage of a system (see column 3 lines 1-20);

transmitting a voltage monitor signal if the voltage falls below a predetermined threshold.

Matsushita discloses transmitting reset signal RS as input of delay circuit (see figure 1 item RS

and column 3 lines 25-27);

transmitting a power delay signal in response to the voltage monitor signal (see figure 1

item TS and column 3 lines 27-30);

transmitting a reset signal if the voltage monitor signal indicated a reset condition or in

response to an external event reset signal. Matsushita discloses a transmitting reset signal RS

when the voltage E drops below a reference voltage, indicating transmitting a reset signal if the

voltage monitor signal indicated a reset condition (see figure 1 item RS and column 3 lines 15-

21);

asserting a system reset signal (see figure 1 item RS and column 3 lines 15-21) and

sending two configuration signals in response to the power delay signal or reset signal, the

configuration signal indicating whether the external event reset signal was detected for at least a predetermined amount of time and at least one of a power failure or an external reset event is detected. Matsushita discloses transmitting TS in response to reset signal RS after a predetermined constant delay time, indicating the external event reset signal was detected for at least a predetermined amount of time and at least one of a power failure (see column 3 lines 27-30) and further discloses transmitting FS in response to reset signal RS indicating the voltage had dropped below the lower voltage limits (see column 4 lines 15-25), indicating at least one of a power failure or an external reset event is detected.

Examiner's Statement of Reason for Allowance

The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 17-20 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts.

The reason for allowance for claim 17 is a memory controller to control and configure the memory sub-system, the memory controller having a power fail controller to receive a power delay signal or a reset signal from the power delay circuit, the power controller asserting a system reset signal and sending two configuration signals in response to the power delay signal or reset signal, the configuration signals indicating whether the external event reset signal was detected for at least a predetermined amount of time and at least one of the power failure or an external reset event is detected in conjunction with the rest of the limitation set forth in the claim.

The remaining claims, not specifically mentioned, are allowed because they are dependent upon one of the claim mentioned above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (571) 272-3652. The examiner will be moving in October 13, 2004. The examiner number at the new site is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Emerson Puente
3/14/05

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
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